



DATA SHEET

GPBA02B

NEW I/O Extender with Constant Current and PWM

Mar. 08, 2024

Version 1.3

GENERALPLUS TECHNOLOGY INC. reserves the right to change this documentation without prior notice. Information provided by GENERALPLUS TECHNOLOGY INC. is believed to be accurate and reliable. However, GENERALPLUS TECHNOLOGY INC. makes no warranty for any errors which may appear in this document. Contact GENERALPLUS TECHNOLOGY INC. to obtain the latest version of device specifications before placing your order. No responsibility is assumed by GENERALPLUS TECHNOLOGY INC. for any infringement of patent or other rights of third parties which may result from its use. In addition, GENERALPLUS products are not authorized for use as critical components in life support devices/systems or aviation devices/systems, where a malfunction or failure of the product may reasonably be expected to result in significant injury to the user, without the express written approval of Generalplus.

Table of Contents

	<u>PAGE</u>
1. GENERAL DESCRIPTION	4
2. FEATURES	4
3. BLOCK DIAGRAM	5
4. SIGNAL DESCRIPTIONS	6
4.1. PAD ASSIGNMENT	7
4.2. PIN MAP	8
4.2.1. LQFP 44 Package Top View	8
4.2.2. LQFP 48 Package Top View	8
5. FUNCTIONAL DESCRIPTIONS	9
5.1. SPI	9
5.1.1. SPI Serial Interface	9
5.1.2. Data Frame Description	9
5.1.3. Command List	9
5.1.4. Waveform of SPI Pin	10
5.2. CONTROL REGISTERS	10
5.2.1. I/O function register	10
5.2.2. New Function Enable Control Register	11
5.2.3. PWMIO Function Control Register	12
5.2.4. Current Sink I/O Control & Software Reset Disable control register	13
5.2.5. CMOS Inverter & Interrupt Control Registers	13
5.3. TIMING DIAGRAM FOR SPI CONTROL	14
5.3.1. I/O Operation Function Timing	14
5.3.2. SPI Synchronous Data Timing Specifications	15
5.4. PORT A/B/C	16
5.4.1. I/O Cell Configuration	17
5.4.2. Combination IO Status to Archive IO Function	17
5.4.3. Special Functions	19
5.5. PWMIO	20
5.5.1. PWMIO Duty Control	20
5.5.2. PWMCK Source Select	21
5.6. PWMIO WITH CONSTANT CURRENT SINK OUTPUT	21
5.6.1. Constant Current Selection	21
5.7. INTERRUPT	21
5.8. CMOS INVERTER	23
5.9. SOFTWARE CONTROL RESET	23
6. ELECTRICAL SPECIFICATION	24
6.1. ITEM DEFINITION	24
6.2. ABSOLUTE MAXIMUM RATINGS	24
6.3. DC CHARACTERISTICS (T _A = 25°C)	25
7. PACKAGE/PAD LOCATIONS	26
7.1. ORDERING INFORMATION	26
7.2. PACKAGE INFORMATION	27

7.2.1. LQFP44.....	27
7.2.2. LQFP48.....	28
8. DISCLAIMER.....	29
9. REVISION HISTORY	30

NEW I/O Extender with Constant Current and PWM

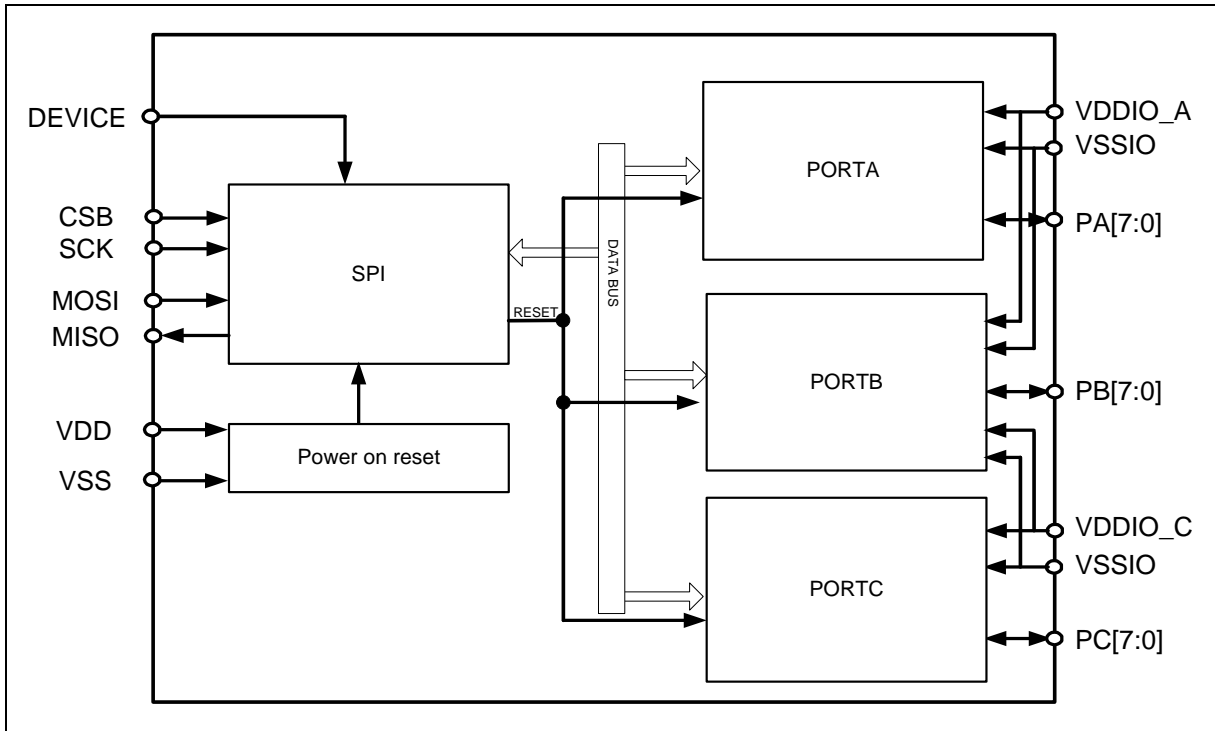
1. GENERAL DESCRIPTION

GPBA02B, a newly invented I/O extender for micro-controller extending I/O pads application, equips with a standard SPI (Mode 0) communication-processing block and 24 I/O ports. With high-speed bit operation of AND/OR/XOR for each bit in internal configuration registers, I/Os' status can be modified within fewer host CPU cycles. These I/Os are provided with strong driving capability to drive LED directly. GPBA02B furnishes 16 PWMIO channels, and there are two sets of constant-current sink function dedicated for these PWMIO channels to use. GPBA02B is fully compatible with GPBA02A.

2. FEATURES

- Operating Voltage
 - Chip operating voltage (VDD): 2.0V – 5.5V
 - I/O operating voltage (VDDIO): 2.0V – 5.5V
- Standard SPI (Mode 0) Interface
 - Four pins for SPI communication
 - Chip Selecting Signal (CSB) as transmitting enable signal
 - Serial clock SCK (max 8MHz) as data synchronization signal for transmitting and receiving data
 - To receive command and data from host via MOSI pin
 - To transmit data to host via MISO pin
- 24 I/Os
 - 24 bi-directional I/O lines
 - Selecting pull high/low resistors or buffer/open-drain outputs via corresponding registers.
 - To execute high-speed AND/OR/XOR function of each bit in I/O configuration registers through writing to the corresponding registers.
- 16 PWMIO Output Channels
 - Sixteen 256-step channels, PA[7:0] and PC[7:0]
- Two sets of constant current sink functions for 16 PWMIO channels
 - Two sets of four-level constant current sink, PA[7:0] and PC[7:0]
- Four CMOS Inverters
 - PB[0] input with PB[1] CMOS inverting output
 - PB[3] input with PB[2] CMOS inverting output
 - PB[4] input with PB[5] CMOS inverting output
 - PB[7] input with PB[6] CMOS inverting output
- Four Interrupt Sources
 - Four interrupt sources (PA[3:0])
 - One output interrupt flag (PA[4])
- Reset Management
 - Power on reset
 - Software control reset

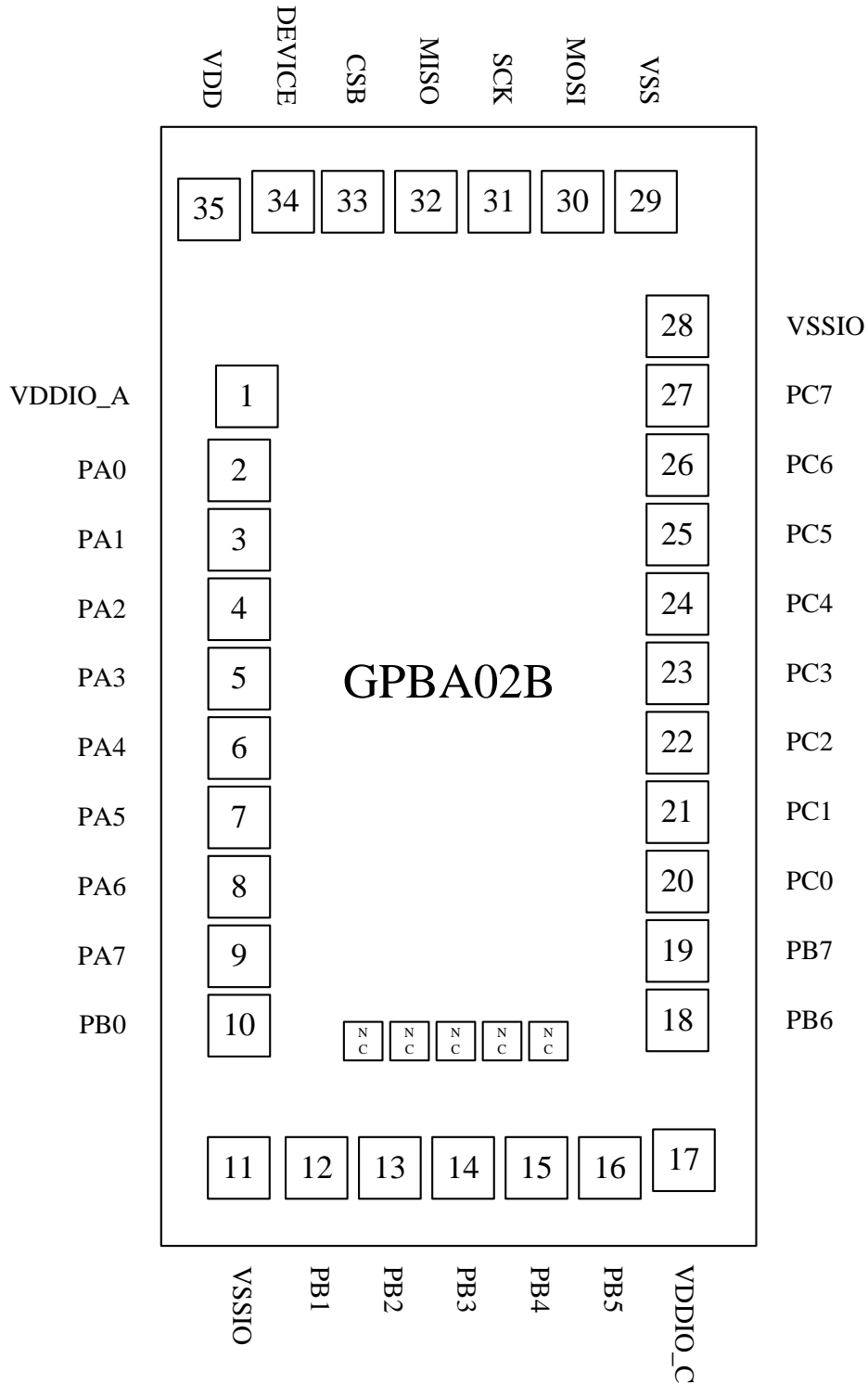
3. BLOCK DIAGRAM



4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Package PIN No.	Type	Description
DEVICE	34	30	I	Device selecting signal, optional. (Device is defaulted as 0 when DEVICE pin is floating)
CSB	33	29	I	Chip selecting signal for SPI interface, low active.
SCK	31	27	I	Clock signal for SPI interface.
MOSI	30	26	I	Data input pin for SPI interface.
MISO	32	28	O	Data output pin for SPI interface.
PA [7:0]	2-9	42-35	I/O	General-purpose inputs/outputs, software command configurable. Pertained to VDDIOA power group.
PB [7:0]	10, 12-16, 18-19	13-12, 8-4, 43	I/O	General-purpose inputs/outputs, software command configurable. PB0 is pertained to VDDIOA power group and PB[7:1] to VDDIOC power group.
PC[7:0]	20-27	21-14	I/O	General-purpose inputs/outputs, software command configurable. Pertained to VDDIOC power group.
VDD	35	31	P	Digital circuit power input.
VSS	29	25	P	Digital circuit ground input.
VDDIO_A	1	34	P	Port A and Port B circuit power input, supply power for PA[7:0] and PB0.
VSSIO	11, 28	3, 22	P	Port A, Port B, Port C circuit ground input.
VDDIO_C	17	9	P	Port B and Port C circuit power input, supply power for PB[7:1] and PC[7:0].

4.1. PAD Assignment



Please connect substrate to VSS or keep floating

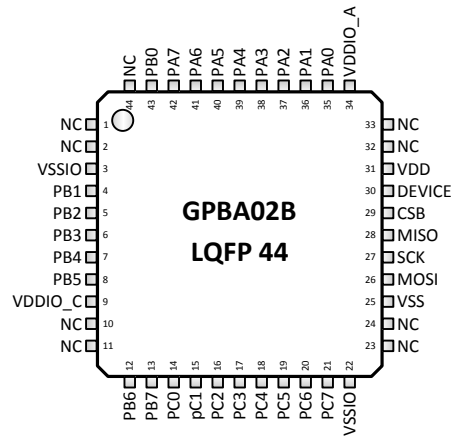
Note1: To ensure IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor located between VDD and VSS should be placed proximately to IC as close as possible.

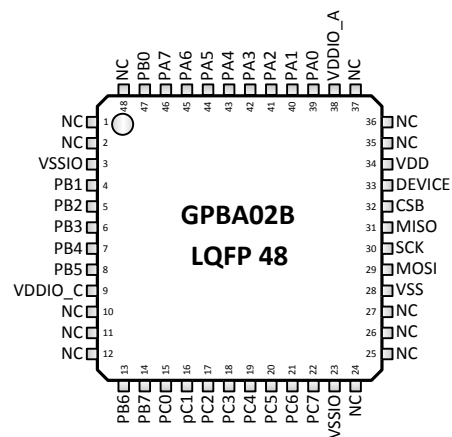
Note3: Please don't bond NC Pins.

4.2. Pin Map

4.2.1. LQFP 44 Package Top View



4.2.2. LQFP 48 Package Top View



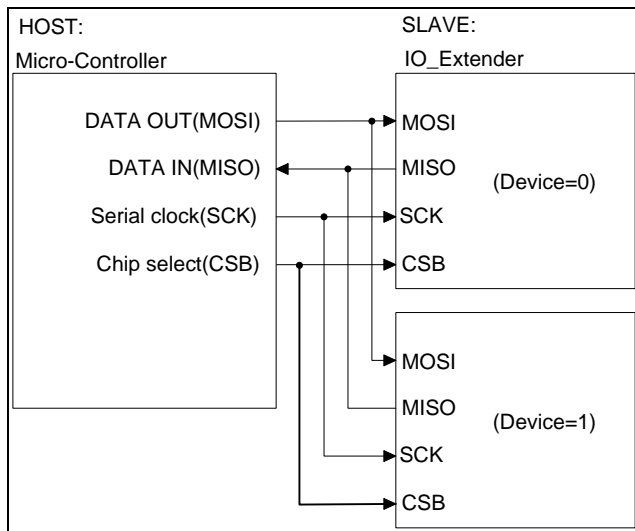
5. FUNCTIONAL DESCRIPTIONS

The I/O extender features 24 I/O ports, which are classified into three groups: Port A, Port B, and Port C. These I/O ports can be configured as normal I/O ports. Also, each port furnishes programmable pull high/low input and open drain output function. Port A and Port C also provide PWMIO output function with current sink output function.

5.1. SPI

The SPI supports full-duplex synchronous transfer between a master device and a slave device. GPBA02B only supports slave mode for SPI transfer (MODE 0).

5.1.1. SPI Serial Interface



As shown in the above diagram, the host can connect two I/O extenders. The device selecting bit is controlled by software command from the host. If the corresponding bit (B6) of the command is set as 0, the apparatus signed with Device=0 will be selected. And else, if the corresponding bit (B6) of the command is set as 1, the apparatus signed with Device=1 is selected. The I/O extender has separated pins designated for data transmission (MISO) and reception (MOSI). When the device is selected and the CSB pin is low, data and command are able to be transmitted via MOSI and MISO pins. When the device is not selected or the CSB pin is not low, data will not be accepted via MOSI pin, and the serial output pin (MISO) will remain at high impedance state. The serial clock pin (SCK) of I/O extender is always set as an input; the I/O extender always operates as a slave.

5.1.2. Data Frame Description

When the host writes data into I/O extender registers, one writing data frame will form 16 bits data. The first 8 bits are command data, and the following 8-bit data will be written into register. The

host sends command and value from MSB to LSB via MOSI pin. During write operation cycles, the MISO pin keeps in high impedance status.

When the host reads data from I/O extender registers or I/O ports, the read command byte will first be sent to I/O extender from MSB to LSB via MOSI pin during the first eight SCK clock cycles. And the value byte read from corresponding register will be sent to host via MISO pin during the following 8 SCK clock cycles from MSB to LSB.

HOST writes data to register:

MOSI	COMMAND	DATAIN
MISO	Z	Z

HOST reads data from register:

MOSI	COMMAND	X
MISO	Z	DATAOUT

5.1.3. Command List

Command	b7(MSB)	b6	b5	b4	b3	b2	b1	b0
Write register	1	1*	Register address					
Read register	0	1*	Register address					
Reset	FFH							
No response	others							

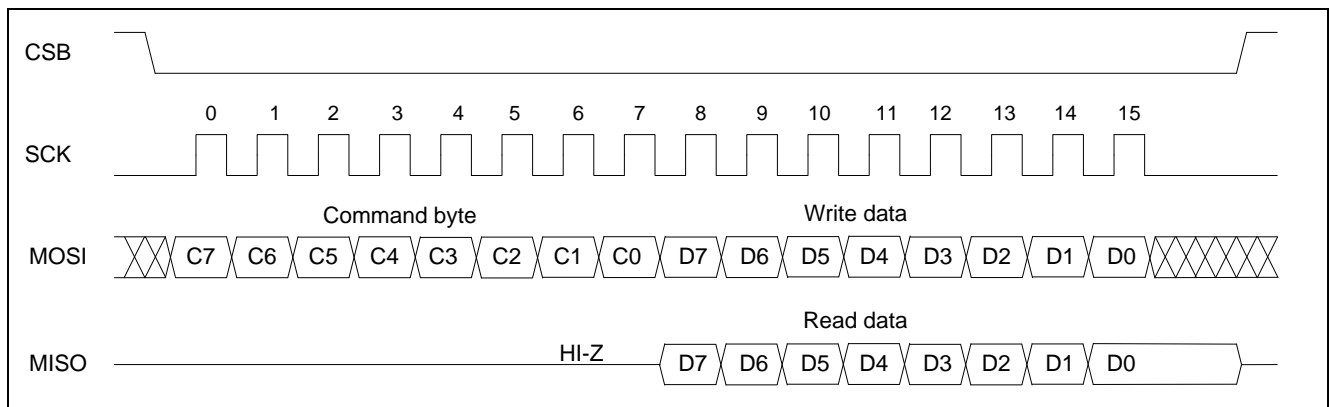
Note: 1* is optional and user can choose device 1 or 0 (two devices) in one SPI interface with bonding option PAD (DEVICE).

As shown in the command list, the read or write command consists of 8-bit data. The highest b7 represents reading or writing operation. When this bit is low, the command executes a read instruction. On the contrary, when this bit is high, the command executes a write instruction. The b6 is used for device selecting and the value depends on the bonding option bit. This option bit should be configured as low or high by users in advance. When DEVICE pin is floating, the value of b0 will be defaulted as 0. If the value of b6 is the same as the option bit, this I/O extender is selected, and this command will be executed. Otherwise, this I/O extender will not respond. The content of b5-0 is used for register address. The reading or writing command is executed for the register with this address. In addition, if the B7-0 of the command is equal to FFH, all those built-in registers will be reset to the initial values. This software command and power-on reset can make all the registers to be reset.

5.1.4. Waveform of SPI Pin

The following diagram shows when the host writes data into or reads data from this I/O extender, it will send a low voltage chip-selecting signal on CSB pin. And the host needs to generate 16 clock pulses on SCK pin for a data frame's synchronization. The CSB should keep in low voltage until this data frame transmission is done (It is suggested the CSB should keep in low voltage at least half a SCK clock cycle after the 16th

pulse). And when the host starts a new data frame transmission, the CSB signal should change from high voltage to low voltage. It means that the CSB cannot maintain in low voltage even if the host transmits two or more data frames continuously. The CSB needs shift to high voltage between every two data frames transmission. The I/O extender receives command-byte and writing-byte via MOSI pin, and transmits reading-byte via MISO pin.



5.2. Control Registers

5.2.1. I/O function register

As shown in the registers list, the address can be represented by 6-bit binary data (supposed to be B [5:0]). For the normal I/O operation, users can write data into address 0xH (B[5:4]=00) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) to achieve various IO functions, and read data from address 0xH (AB5-4=00) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) and ports (DATA/B/C) to obtain register and IO ports states.

special designed registers that is able to reduce the operation time. For instance, writing data to address 1xH (AB5-4=01) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) will accelerate AND operation for the corresponding 0xH registers, or writing data to address 2xH (AB5-4=10) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) will speed up the OR operation for the corresponding 0xH registers. Similarly, writing data to address 3xH (AB5-4=11) registers (BUFA/B/C, DIRA/B/C and ATTA/B/C) accelerates the XOR operation for the corresponding 0xH registers.

In order to accelerate I/O operation, GPBA02B features some

Control registers list:

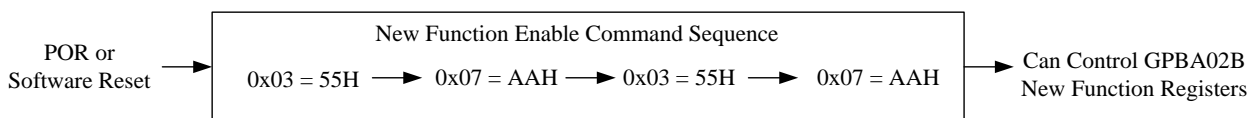
Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
IO Port	00H(R/W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFA	00
	01H(R/W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFB	00
	02H(R/W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFC	00
	04H(R/W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRA	00
	05H(R/W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRB	00
	06H(R/W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRC	00
	08H(R/W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTA	00
	09H(R/W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTB	00
	0AH(R/W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTC	00
	0CH(R)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DATA	--
	0DH(R)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DATB	--
	0EH(R)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DATC	--

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
AND Group	10H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFA AND	--
	11H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFB AND	--
	12H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFC AND	--
	14H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRAAND	--
	15H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRBAND	--
	16H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRCAND	--
	18H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTAAND	--
	19H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTBAND	--
	1AH(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTCAND	--
OR Group	20H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFAOR	--
	21H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFBOR	--
	22H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFCOR	--
	24H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRAOR	--
	25H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRBOR	--
	26H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRCOR	--
	28H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTAOR	--
	29H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTBOR	--
	2AH(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTCOR	--
XOR Group	30H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BUFAXOR	--
	31H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	BUFBXOR	--
	32H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	BUFCXOR	--
	34H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	DIRAXOR	--
	35H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	DIRBXOR	--
	36H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	DIRCXOR	--
	38H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	ATTAXOR	--
	39H(W)	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	ATTBXOR	--
	3AH(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	ATTCXOR	--

5.2.2. New Function Enable Control Register

Address 03H and 07H are GPBA02B's new function enabling registers. Users must follow the command sequence, shown in the following figure, before setting the control registers listed in 5.2.3 ~ 5.2.5. This command sequence only needs to be executed once unless it needs to be executed again after the

POR or software reset. In this way, all PWMIO, Constant Current Sink, CMOS Inverter, and Interrupt corresponding registers can be set. However, there is no need to execute the command sequence before setting the I/O corresponding registers in 5.2.1.



Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
Function Enable control	03H(W)	0	1	0	1	0	1	0	1	03H = 55H	00
	07H(W)	1	0	1	0	1	0	1	0	07H = AAH	00

5.2.3. PWMIO Function Control Register

Address 17H is PA7~PA0 PWMIO's enable control register, where PA7~PA0 PWMIO can be enabled individually. Setting B7~B0 of address 17H as "1" to enable PA7~PA0 PWMIO channels.

Address 1CH~1FH and 2BH~2EH are PA0~PA7's PWMIO duty control registers.

Address 27H is PC7~PC0's PWMIO enable control registers, where PC7~PC0 PWMIO can be enabled individually. Setting

B7~B0 of address 27H as "1" to enable PC7~PC0 PWMIO channels.

Address 2FH, 33H, 37H, and 3BH~3FH are PC0~PC7's PWMIO duty control registers.

Address 1BH is PWMCK source register. Setting PA_DIV2~0 and PC_DIV2~0 registers can control the frequency of PA PWMCK and PC PWMCK.

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
PA PWMIO	17H(W)	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	PA7~PA0 PWMIO enable control	00
	1CH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA0 Duty	00
	1DH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA1 Duty	00
	1EH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA2 Duty	00
	1FH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA3 Duty	00
	2BH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA4 Duty	00
	2CH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA5 Duty	00
	2DH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA6 Duty	00
2EH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PA7 Duty	00	

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
PC PWMIO	27H(W)	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	PC7~PC0 PWMIO enable control	00
	2FH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC0 Duty	00
	33H(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC1 Duty	00
	37H(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC2 Duty	00
	3BH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC3 Duty	00
	3CH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC4 Duty	00
	3DH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC5 Duty	00
	3EH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC6 Duty	00
3FH(W)	DUTY7	DUTY6	DUTY5	DUTY4	DUTY3	DUTY2	DUTY1	DUTY0	PC7 Duty	00	

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
PWMCK	1BH(W)	--	PA_DIV2	PA_DIV1	PA_DIV0	--	PC_DIV2	PC_DIV1	PC_DIV0	PA PC PWMIO clock source control	00

5.2.4. Current Sink I/O Control & Software Reset Disable control register

Address 13H is Software Reset control registers and Current Sink control registers. Set B7 of address 13H as “1” to disable Software reset so that FFH command reset will be invalid. Setting B6 as “1” can enable PC constant current sink for PC PWMIO channels, and

set B2 as “1” can enable PA constant current sink for PA PWMIO channels. In addition, setting PC_CR_SEL1~0 and PA_CR_SEL1~0 to adjust the 4-levels constant-current.

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
Current Sink	13H(W)	software reset disabled	PC CR_EN	PC CR_SEL1	PC CR_SEL0	--	PA CR_EN	PA CR_SEL1	PA CR_SEL0	Software reset control & current Sink control register	00

5.2.5. CMOS Inverter & Interrupt Control Registers

Address 0BH is Interrupt flag and interrupt enable control register. Set B3~B0 as “1” to enable interrupt and write B7~B4 to clear interrupt flag3~0. Users can also read address 0BH to obtain interrupt status.

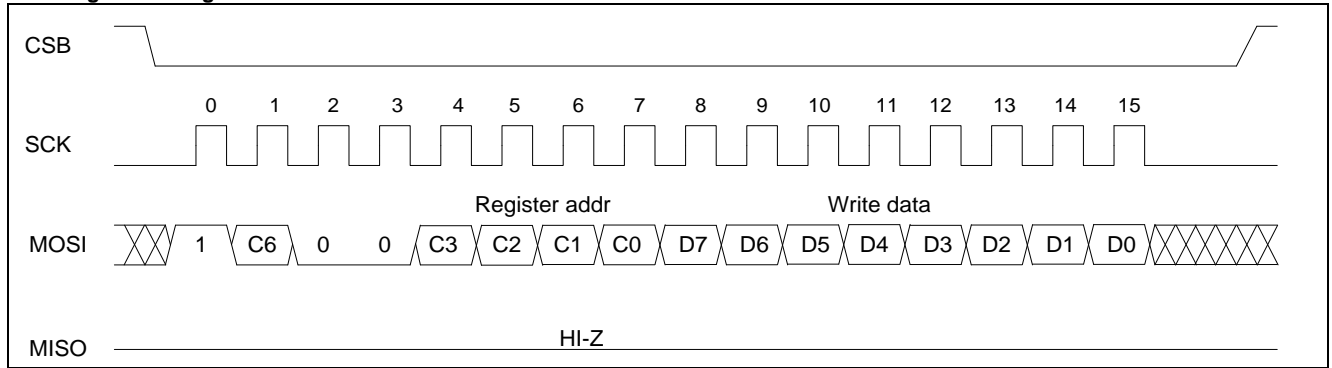
Address 23H is interrupt edge control and CMOS inverter enable control register. Setting INT_EDGE3~0 registers can select rising edge trigger interrupt or falling edge trig interrupt. Users can set B3~B0 as “1” to enable I/O for CMOS inverter application.

Function	Address	B7	B6	B5	B4	B3	B2	B1	B0	Comment	Default
Interrupt & CMOS inverter	0BH(R/W)	INT FLAG3	INT FLAG2	INT FLAG1	INT FLAG0	INT EN3	INT EN2	INT EN1	INT EN0	Interrupt flag & enable control	00
	23H(W)	INT EDGE3	INT EDGE2	INT EDGE1	INT EDGE0	CMOS EN3	CMOS EN2	CMOS EN1	CMOS EN0	Interrupt edge & CMOS enable control	00

5.3. Timing Diagram for SPI Control

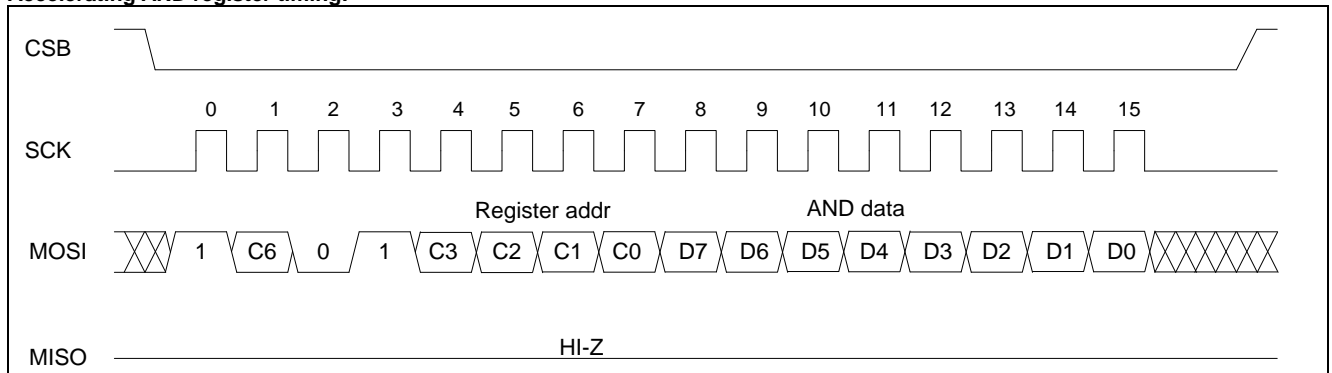
5.3.1. I/O Operation Function Timing

Write register timing:



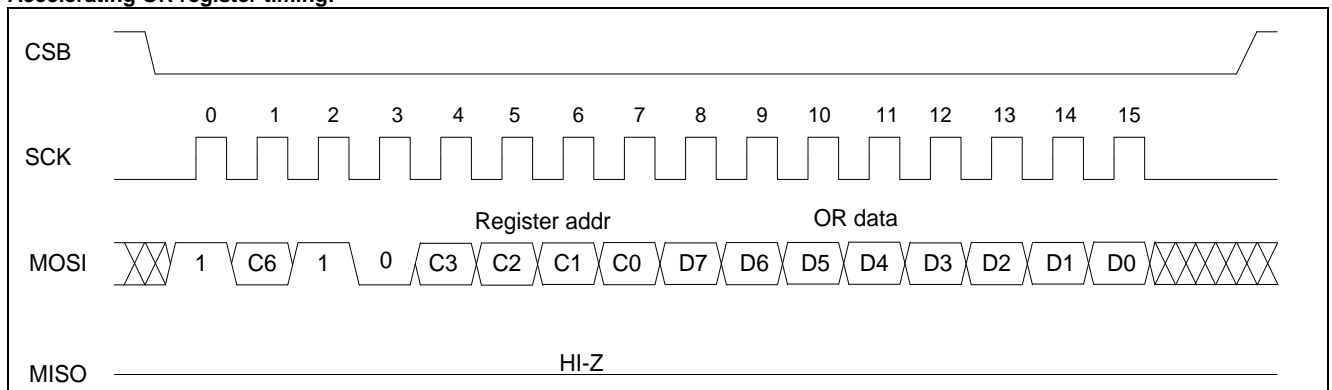
The command byte: C7=1; C6=device option value; C5-4=00; C3-0=register address. The write data byte: D7-0 is the value that will be written to the corresponding register. In writing register cycles, the output pin (MISO) remains in high impedance state.

Accelerating AND register timing:



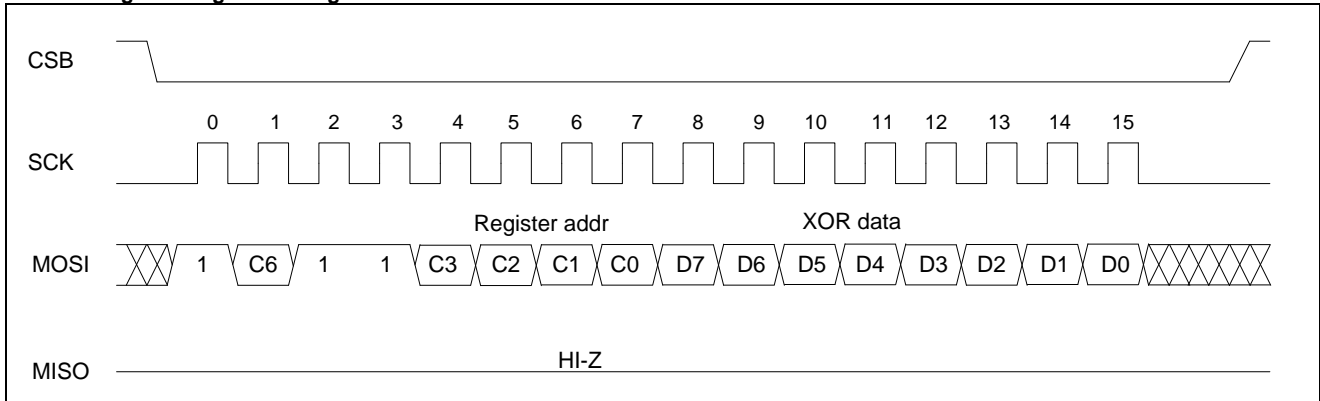
The command byte: C7=1; C6=device option value, C5-4=01, C3-0=register address. The accelerating AND data byte: D7-0 is the value that will be AND with the corresponding 0xH register's value, and then written to the corresponding 0xH register. To accelerate AND register cycles, the output pin (MISO) remains at high impedance state.

Accelerating OR register timing:



The command byte: C7=1; C6=device option value; C5-4=10; C3-0=register address. The accelerating OR data byte: D7-0 is the value that will be OR with the corresponding 0xH register's value, and then written to the corresponding 0xH register. To accelerate OR register cycles, the output pin (MISO) remains at high impedance state.

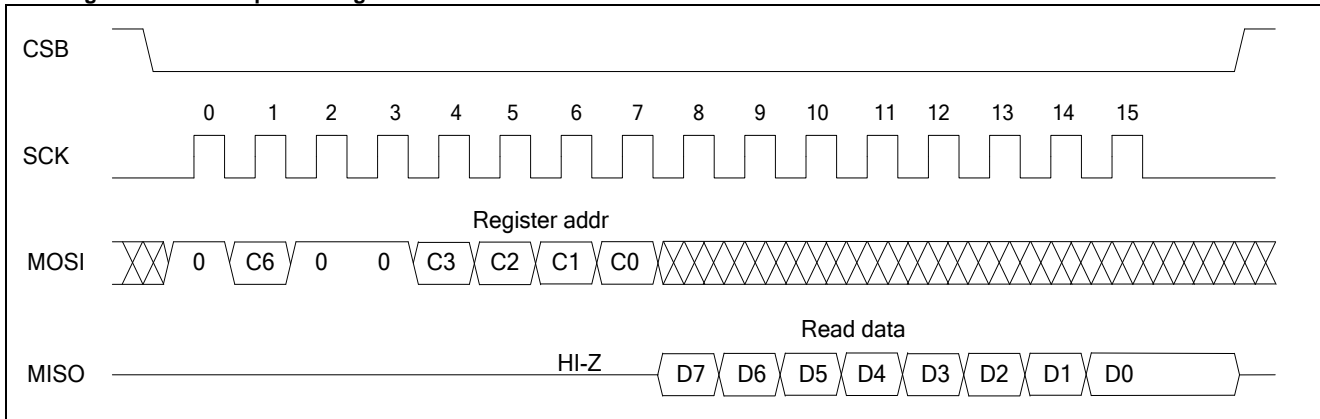
Accelerating XOR register timing:



The command byte: C7=1; C6=device option value; C5-4=11; C3-0=register address. The accelerating XOR data byte: D7-0 is the value that will be XOR with the corresponding 0xH register's

value, and then written to the corresponding 0xH register. To accelerate XOR register cycles, the output pin (MISO) remains at high impedance state.

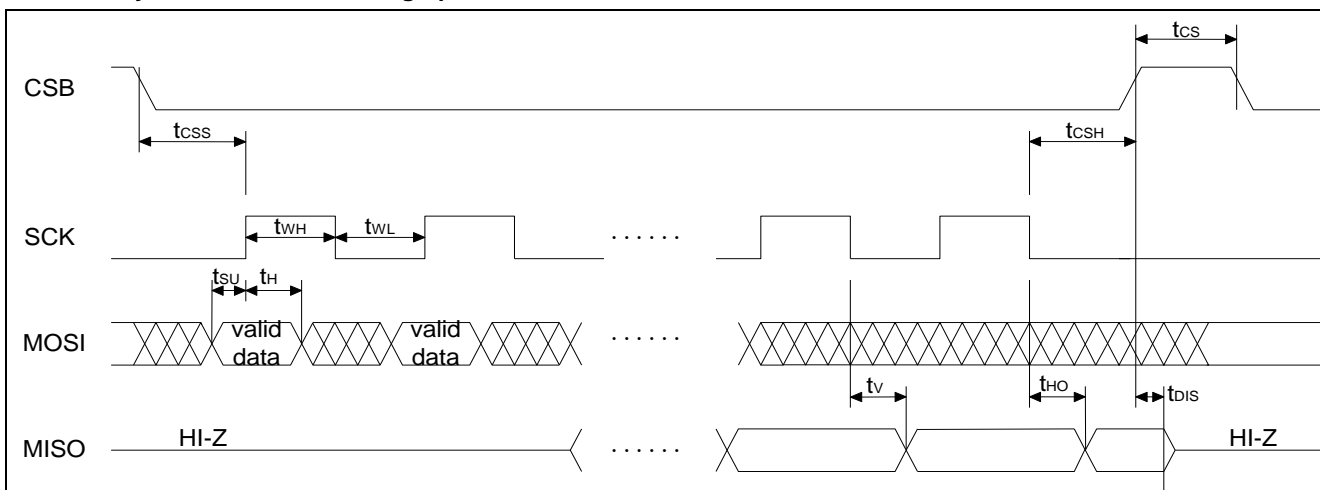
Read register or read IO port timing:



The command byte: C7=0, C6=device option value, C5-4=00, C3-0=register address. The read data byte: D7-0 is the value that will be read from the corresponding register or corresponding IO ports. In read register or IO port cycles, the read data byte is

transmitted via output pin (MISO) during the last 8 SCK clock cycles. After the 16th SCK clock, MISO remains the value of B0 until CSB is high.

5.3.2. SPI Synchronous Data Timing Specifications



Symbol	Parameter	Min.	Typ.	Max.	Units
f _{SCK}	SCK Clock Frequency	-	-	8	MHz
t _{WH}	SCK High Time	58.5	-	-	ns
t _{WL}	SCK Low Time	58.5	-	-	ns
t _{CS}	CSB Setup Time	80	-	-	ns
t _{CSH}	CSB Hold Time	80	-	-	ns
t _{CS}	CSB High Time	50	-	-	ns
t _{SU}	Data In Setup Time	5	-	-	ns
t _H	Data In Hold Time	5	-	-	ns
t _V	Output Valid	-	-	57	ns
t _{HO}	Output Hold Time	0	-	-	ns
t _{DIS}	Output Disable Time	0	-	-	ns

5.4. Port A/B/C

In Port A, Port B, and Port C, each has eight programmable I/Os that are controlled by data register BUFA/B/C, direction control register DIRA/B/C, and attribution control register ATTA/B/C. BUFA/B/C is used to store the data content for output. Reading DATA/B/C will get pad's status and latch current's status into internal latching register.

There is a built-in pull-high/low resistor on each pad. PA/B/C [7:0] has pull-high/low resistors that can be configured with pull-high or pull-low registers. These pull-high/low resistors can be selected by I/O configuration register (BUFA/B/C, DIRA/B/C, and ATTA/B/C).

The corresponding pads are assigned for GPBA02B as following:

PIN	Pull High/Low Resistance@VDDIO=5V	IN	OUT Current @VDDIO=3V
PA7	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA6	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA5	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA4	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA3	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA2	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA1	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PA0	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB7	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB6	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB5	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB4	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB3	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB2	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB1	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PB0	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC7	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC6	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC5	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC4	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC3	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC2	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA
PC1	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA

PIN	Pull High/Low Resistance@VDDIO=5V	IN	OUT Current @VDDIO=3V
PC0	100K High/Low	Schmitt-Trigger(0.4/0.6 VDD)	-8/20mA

5.4.1. I/O Cell Configuration

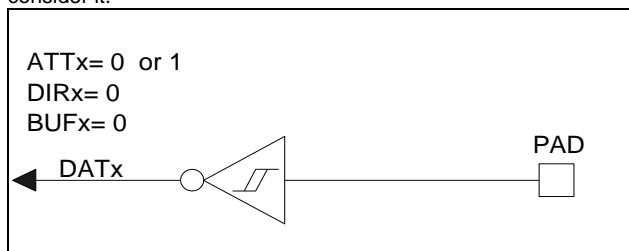
Mode: output high, output low, input with PL, input with PH, input with high Z, open drain NMOS output, open drain PMOS output.

5.4.2. Combination IO Status to Archive IO Function

ATT _x	DIR _x	BUF _x	IO status	Function
0	0	0	Floating(default)	Floating input
0	0	1	Pull low	Pull low input
1	0	1	Pull high	Pull high input
0	1	0	Output low	Buffer output
0	1	1	Output high	
1	0	0	Floating	Open drain P-MOS output
1	1	0	Output high	
1	0	1	Pull high	Wire AND (inverted)
1	1	1	Output low	
0	1	0	Output low	Open drain N-MOS output (inverted)
0	0	0	Floating	
0	0	1	Pull low	Wired OR
0	1	1	Output high	
0	0	0	Floating	Dynamic pull low input
0	0	1	Pull low	
1	0	0	Floating	Dynamic pull high input
1	0	1	Pull high	
1	1	0	Output high	Inverted buffer output
1	1	1	Output low	

Input with high Z:

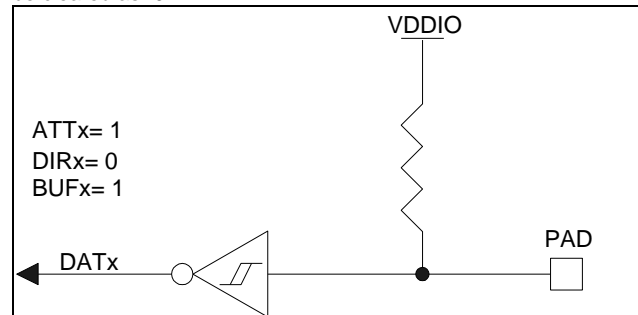
As shown in the above I/O Cell Configuration table and Control Registers table, the default values of all these registers are 0. And the default states of all these I/O ports are input with high Z. If PA/B/Cx is expected to set as input with high Z port (floating), the corresponding Bx of 00H/01H/02H (BUFA/B/C) and 04H/05H/06H (DIRA/B/C) both should be cleared as "0". In this case, the values of corresponding ATTA/B/Cx bit do not have to consider it.



Input with pull high resistor (PH):

As shown in the above I/O Cell Configuration table and Control

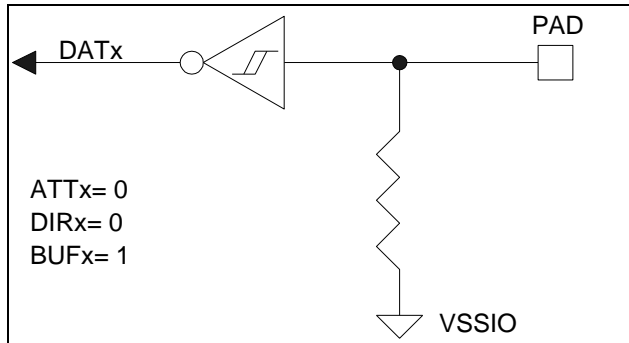
Registers table, each I/O port can be set as Input with pull high resistor port independently. If PA/B/Cx is expected to set as Input with pull high resistor port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) and 08H/09H/0AH (ATTA/B/C) both should be set as "1", and the corresponding Bx of 04H/05H/06H (DIRA/B/C) should be cleared as "0".



Input with pull low resistor (PL):

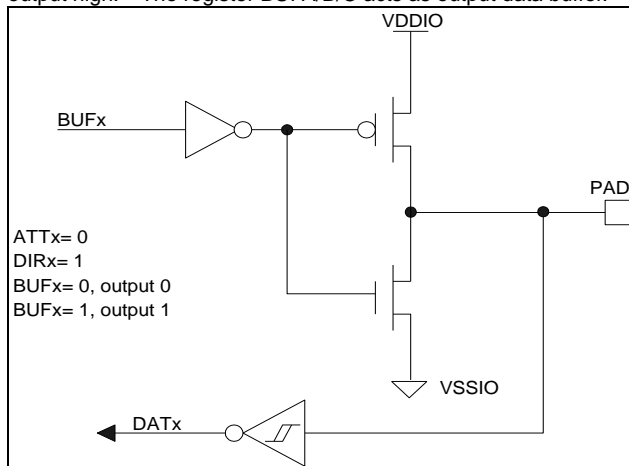
As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as Input with pull low

resistor port independently. If PA/B/Cx is expected to set as Input with pull low resistor port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) should be set as "1", and the corresponding Bx of 04H/05H/06H (DIRA/B/C) and 08H/09H/0AH (ATTA/B/C) both should be cleared as "0".



CMOS output high/low:

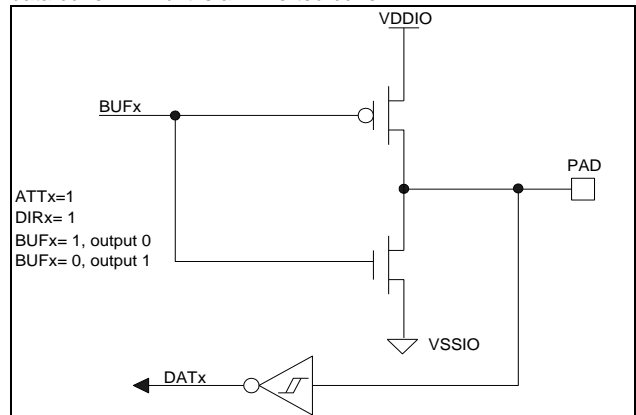
As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as CMOS output port independently. If PA/B/Cx is expected to set as CMOS output port, the corresponding Bx of 08H/09H/0AH (ATTA/B/C) should be configured as "0", and the corresponding Bx of 04H/05H/06H (DIRA/B/C) should be configured as "1". In addition, if the host writes 0 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the PA/B/Cx will output low. And else if the host writes 1 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the PA/B/Cx will output high. The register BUFA/B/C acts as output data buffer.



Inverted CMOS output high/low:

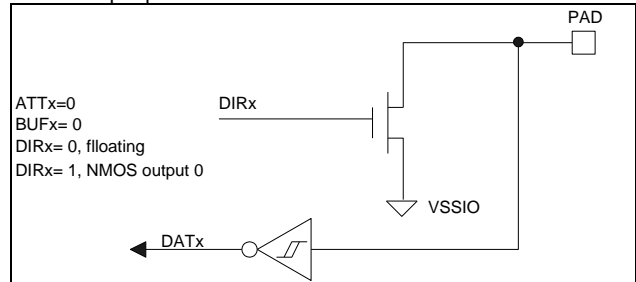
As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as CMOS output port independently. If PA/B/Cx is expected to set as CMOS output port, the corresponding Bx of 08H/09H/0AH (ATTA/B/C) and 04H/05H/06H (DIRA/B/C) should be configured as 1. In addition, if the host writes 0 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the PA/B/Cx will output high. And else, if the host writes 1 to corresponding Bx of 00H/01H/02H (BUFA/B/C), the

PA/B/Cx will output low. The register BUFA/B/C acts as output data buffer. And it is an inverted buffer.



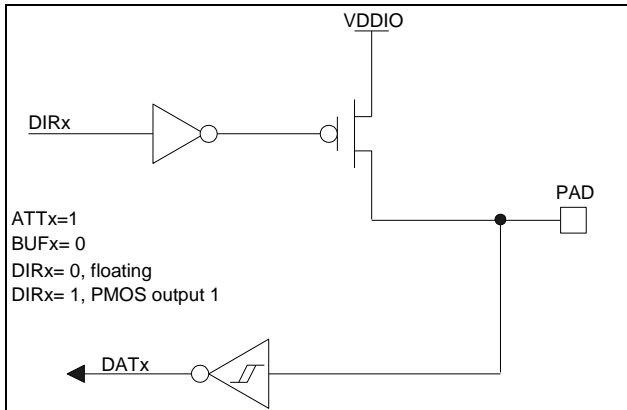
Inverted open drain NMOS output:

As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as open drain NMOS output port independently. If PA/B/Cx is expected to set as open drain NMOS output port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) and 08H/09H/0AH (ATTA/B/C) should be cleared as "0", and then if the host writes "1" to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx will output low. And if the host writes 0 to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx is floating. In this case, the register DIRx acts as the output data buffer register. And it is an inverted open drain NMOS output port.



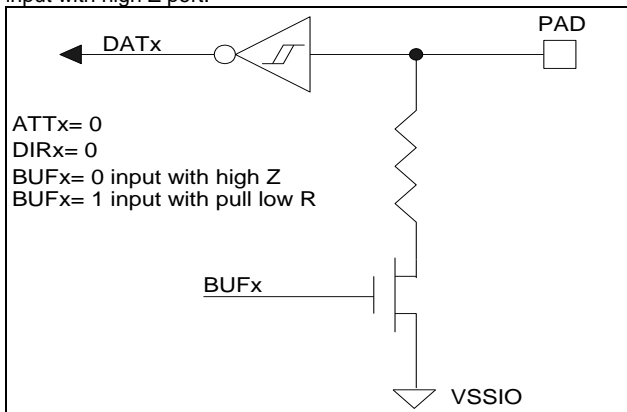
Open drain PMOS output:

As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as open drain NMOS output port independently. If PA/B/Cx is expected to be set as open drain PMOS output port, the corresponding Bx of 00H/01H/02H (BUFA/B/C) should be cleared as "0", and 08H/09H/0AH (ATTA/B/C) should be set as "1". If the host write "1" to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx is an open drain PMOS output, and if host write "0" to the corresponding Bx of 04H/05H/06H (DIRA/B/C), the PA/B/Cx is floating. In this case, the register DIRx acts as the output data buffer register. And it is a normal open drain PMOS output port.



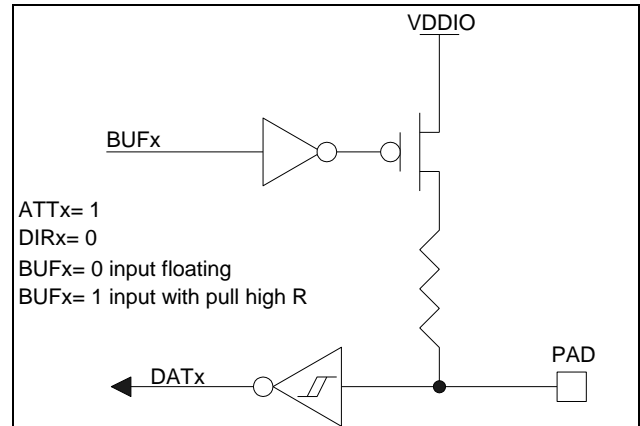
Dynamic pull low input:

As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as dynamic Input with pull low resistor port independently. If PA/B/Cx is expected to set as dynamic Input with pull low resistor port, the corresponding Bx of 04H/05H/06H (DIRA/B/C) and 08H/09H/0AH (ATTA/B/C) both should be cleared as "0". If the corresponding Bx of 00H/01H/02H (BUFA/B/C) is set as "1", the PA/B/Cx is set as input with pull low resistor port, and else if the corresponding Bx of 00H/01H/02H (BUFA/B/C) is cleared as "0", the PA/B/Cx is set as input with high Z port.



Dynamic pull high input:

As shown in the above I/O Cell Configuration table and Control Registers table, each I/O port can be set as dynamic Input with pull high resistor port independently. If PA/B/Cx is expected to set as dynamic Input with pull high resistor port, the corresponding Bx of 04H/05H/06H (DIRA/B/C) should be cleared as "0". And the corresponding Bx of 08H/09H/0AH (ATTA/B/C) should be set as "1". If the corresponding Bx of 00H/01H/02H (BUFA/B/C) is set as "1", the PA/B/Cx is set as input with pull high resistor port, and else if the corresponding Bx of 00H/01H/02H (BUFA/B/C) is cleared as "0", the PA/B/Cx is set as input with high Z port.



Note: Also, there are some other I/O register status combinations that can archive other IO functions, such as wired OR and wired AND functions. Users can use these functions dexterously.

5.4.3. Special Functions

Register to accelerate AND function:

The content of ATTA/B/C, BUFA/B/C and DIRA/B/C can accelerate AND with any data by executing a special write instruction. According to the command data frame, when user writes data into register address of 1xH (B5-4 of command is 01), the writing data will be AND with the current data of this register and then be load in the exact register again. While executing AND instruction, the I/O extender reads the primary value of the register. This accelerating AND operation only spends the host a write command cycle. It is a very useful function for I/Os' real time control.

Register to accelerate OR function:

The content of ATTA/B/C, BUFA/B/C and DIRA/B/C can accelerate OR with any data by executing a special write instruction. According to the command data frame, when user writes data into register address of 2xH (B5-4 of command is 10), the writing data will be OR with the current data of this register and then be load in the exact register again. While executing OR instruction, the I/O extender reads the primary value of the register. This accelerating OR operation only spends the host a write command cycle. It is a very useful function for I/Os' real time control.

Register to accelerate XOR function:

The content of ATTA/B/C, BUFA/B/C and DIRA/B/C can accelerate XOR with any data by executing a special write instruction. According to the command data frame, when user writes data into register address of 3xH (B5-4 of command is 11), the writing data will be XOR with the current data of this register and then be load in the exact register again. While executing XOR instruction, the I/O extender reads the primary value of the register. This accelerating XOR operation only spends the host a write command cycle. It is a very useful function for I/Os' real time control.

Comparing traditional AND/OR/XOR operation with AND/OR/XOR acceleration operation
(Reference by 6502 assembler):

	Traditional	Accelerated
AND Operation	Read a byte from I/O extender → MCU internal "AND" → Write a byte to I/O extender (Example: LDX #\$01 JSR READ_SPI AND #\$55 JSR WRITE_SPI)	Write a byte to "AND" address (Example: LDA #\$55 LDX #\$11 JSR WRITE_SPI)
OR Operation	Read a byte from I/O extender → MCU internal "OR" → Write a byte to I/O extender (Example: LDX #\$01 JSR READ_SPI OR #\$55 JSR WRITE_SPI)	Write a byte to "OR" address (Example: LDA #\$55 LDX #\$21 JSR WRITE_SPI)
XOR Operation	Read a byte from I/O extender → MCU internal "XOR" → Write a byte to I/O extender (Example: LDX #\$01 JSR READ_SPI XOR #\$55 JSR WRITE_SPI)	Write a byte to "XOR" address (Example: LDA #\$55 LDX #\$31 JSR WRITE_SPI)

Note: The sub routine READ_SPI and WRITE_SPI depends on the host structure, it takes at least 34 IO access cycles (enable*2+data_clock*8*2*2, no include data and flow control process) while using software to generate SPI waveform.

5.5. PWMIO

GPBA02B support 16 channels PWMIO output (PA[7:0] PC[7:0]).
 Each PWMIO channel has 256-level control. There are two sets of
 PWMCK using in PA PWMIO channels and PC PWMIO channels

respectively. PWMCK of PA PWMIO channels and PWMCK of PC
 PWMIO channels also have eight adjustable frequencies.

5.5.1. PWMIO Duty Control

PA ATT _x or PC ATT _x	Duty7~Duty0	PWM Output Duty
0	00000000	0
0	00000001	1/256
0	00000010	2/256
0	00000011	3/256
0	--	--
0	01111111	127/256
0	10000000	129/256
0	--	--
0	11111110	255/256
0	11111111	1
1	00000000	1
1	00000001	255/256
1	00000010	254/256

PA ATT _x or PC ATT _x	Duty7~Duty0	PWM Output Duty
1	00000011	253/256
1	--	--
1	01111111	129/256
1	10000000	127/256
1	--	--
1	11111110	1/256
1	11111111	0

As show in the above duty control table, each PWMIO channel has 256-level; users can write each channel duty control registers

to achieve different duty from 0%~100%. The Duty also can be reversed by setting ATT_x as "1".

5.5.2. PWMCK Source Select

PA_DIV2~0	PA_PWMCK	PC_DIV2~0	PC_PWMCK
000	11Mhz	000	11Mhz
001	(11M/2)hz	001	(11M/2)hz
010	(11M/4)hz	010	(11M/4)hz
011	(11M/16)hz	011	(11M/16)hz
100	(11M/32)hz	100	(11M/32)hz
101	(11M/64)hz	101	(11M/64)hz
110	(11M/128)hz	110	(11M/128)hz
111	(11M/256)hz	111	(11M/256)hz

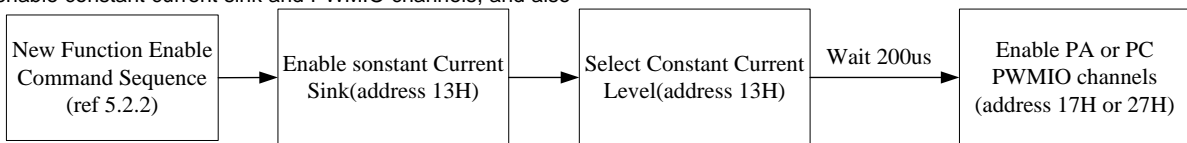
As show in the above table, PWMCKs have PA_PWMCK used in PA PWMIO channels and PC_PWMCK used in PC PWMIO channels. The frequency of PA_PWMCK and PC_PWMCK can be

controlled by PA_DIV2~0 and PC_DIV2~0 registers. Users write corresponding data into PA_DIV2~0 registers and PC_DIV2~0 registers to select the frequency of PA_PWMCK and PC_PWMCK.

5.6. PWMIO with Constant Current Sink Output

PWMIO can output with constant current sink. Note that users must enable constant current sink and PWMIO channels, and also

follow the enabling sequence depicted below:



5.6.1. Constant Current Selection

PA_CR_SEL1~0	PA Channel Constant Current	PC_CR_SEL1~0	PC Channel Constant Current
00	29mA	00	29mA
01	22mA	01	22mA
10	15mA	10	15mA
11	7mA	11	7mA

As shown in the above table, there are two sets of constant current in PA channel and PC channel. Users write corresponding data into PA_CR_SEL1~0 registers and

PC_CR_SEL1~0 registers to select the sink current of PA channels and PC channels respectively.

5.7. Interrupt

There are four interrupt sources available and configured in PA[3:0]. The PA[4] outputs high if interrupt is triggered. Users

can read address 0BH interrupt flags to obtain which interrupt is triggered. As shown in the table below, users can write

corresponding data into INT_EDGE3~0 to achieve which edge to trigger interrupt.

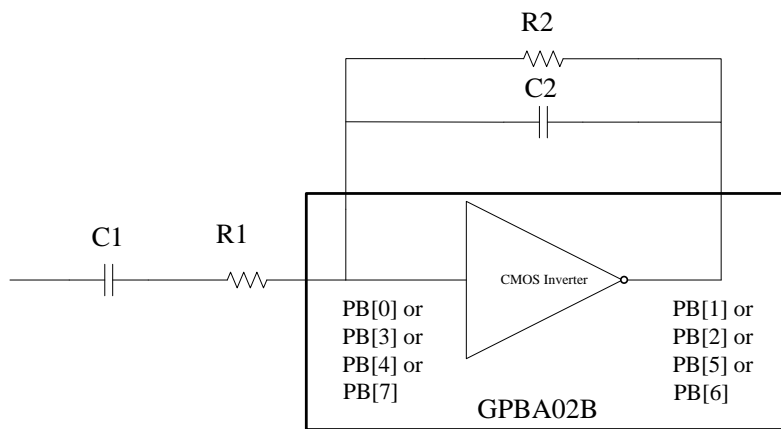
INT_EDGE0	0	PA[0] rising edge trigger interrupt
	1	PA[0] falling edge trigger interrupt
INT_EDGE1	0	PA[1] rising edge trigger interrupt
	1	PA[1] falling edge trigger interrupt
INT_EDGE2	0	PA[2] rising edge trigger interrupt
	1	PA[2] falling edge trigger interrupt
INT_EDGE3	0	PA[3] rising edge trigger interrupt
	1	PA[3] falling edge trigger interrupt

5.8. CMOS Inverter

GPBA02B has four CMOS inverters, and each CMOS inverter shares with PB IO ports. If CMOS inverter function is enabled, PB IO ports will be disabled. The following table shows the

relationships between input pins and CMOS Inverter Output Pins, where CMOS Inverters can be used for amplifier application. The application circuit shows as follows.

Input Pins	CMOS Inverter Output Pins
PB[0] input	PB[1] inverse output
PB[3] input	PB[2] inverse output
PB[4] input	PB[5] inverse output
PB[7] input	PB[6] inverse output



5.9. Software Control Reset

If the b7-b0 of the SPI command is equal to FFH, all registers will be reset to the initial values. If writing PC7 PWMIO duty control register, SPI command byte is also FFH if device is 1. Thus, users must disable Software Reset before writing PC7 PWMIO

duty control registers. The software reset is disabled when b7 of address 1Bh is 1, software reset is enabled when B7 of address 1Bh is 0.

6. ELECTRICAL SPECIFICATION

6.1. Item Definition

Symbol	Definition	Symbol	Definition
V_{IH}	Input High Voltage	R_{LOW}	Pull low Resistor value
V_{IL}	Input Low Voltage	I_{OH}	Output High Current (Source)
I_{OP}	Operation Voltage	I_{OL}	Output Low Current (Sink)
R_{HIGH}	Pull high Resistor value	I_Z	Output Leakage Current (Source)

6.2. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +85°C
I/O Total MAX Current	I_M	-150mA/300mA
LQFP44 Thermal resistance Junction to Case	θ_{JC}	20°C/W
LQFP44 Thermal resistance Junction to Ambient	θ_{JA}	55°C/W
LQFP48 Thermal resistance Junction to Case	θ_{JC}	27°C/W
LQFP48 Thermal resistance Junction to Ambient	θ_{JA}	71°C/W

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause permanent damage to the device. For normal operational conditions, please see DC Electrical Characteristics.

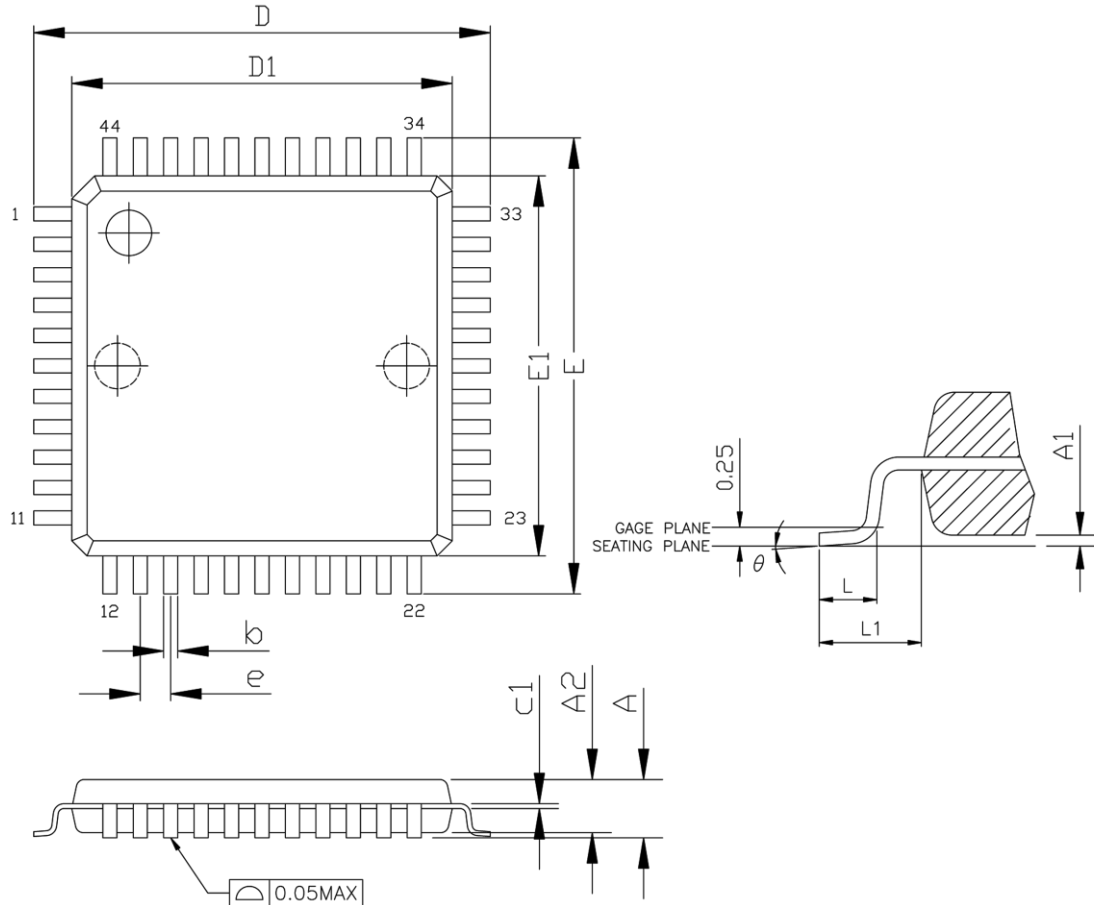
6.3. DC Characteristics (T_A = 25°C)

Characteristics	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Operating Voltage1	VDDIO_A	2.0	-	5.5	V	-
Operating Voltage2	VDDIO_C	2.0	-	5.5	V	-
Operating Voltage3	VDD	2.0	-	5.5	V	-
Operating Current -1	I _{OP1}	-	-	100	μA	VDDIO_X, VDD=5.5V, SCK=8MHz All PWMIO and Constant Current Sink off
Operating Current -2	I _{OP2}	-	4.0	-	mA	VDDIO_X, VDD=5.5V, SCK=8MHz All PWMIO and Constant Current Sink On
Standby Current	I _{STB}	-	-	1.5	μA	VDDIO_X, VDD=5.5V, CSB=VDD
Input High Voltage (PA[7:0], PB[7:0], PC[7:0])	V _{IH}	0.7*VDDIO_X	-	-	V	VDDIO_X = 3.0V
Input Low Voltage (PA[7:0], PB[7:0], PC[7:0])	V _{IL}	-	-	0.3*VDDIO_X	V	VDDIO_X = 3.0V
Output High Voltage (PA[7:0], PB[7:0], PC[7:0])	V _{OH}	2.5	-	-	V	VDDIO_X = 3.0V I _{OH} = -8mA
Output Sink Voltage (PA[7:0], PB[7:0], PC[7:0])	V _{OL}	-	-	0.5	V	VDDIO_X = 3.0V I _{OL} = 20mA
Pull High Resistor (PA[7:0], PB[7:0], PC[7:0])	R _{HIGH}	-	100	-	kΩ	VDDIO_X = 5.0V
Pull Low Resistor (PA[7:0], PB[7:0], PC[7:0])	R _{LOW}	-	100	-	kΩ	VDDIO_X = 5.0V
Constant Current Sink Deviation for Chip	I _{SINK}	-10	-	10	%	VDDIO_X = 3.6V, Vol = 0.8V
Constant Current Sink Deviation for Package	I _{SINK}	-15	-	15	%	VDDIO_X = 3.6V, Vol = 0.8V

7. PACKAGE/PAD LOCATIONS**7.1. Ordering Information**

Product Number	Package Type
GPBA02B-C	Chip form
GPBA02B-QL01x	Green Package - LQFP 44 RoHS
GPBA02B-QL23x	Green Package - LQFP 48 RoHS

Note1: x = 1 - 9, serial number.

7.2. Package Information
7.2.1. LQFP44


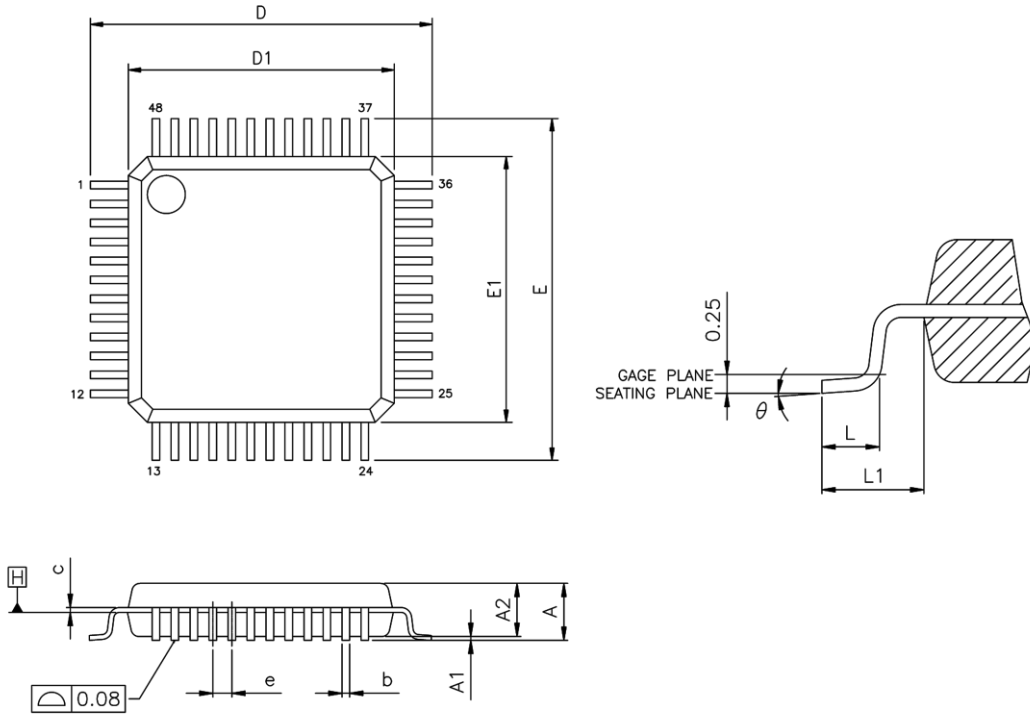
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.60
A1	0.05	–	0.15
A2	1.35	1.40	1.45
c1	0.09	–	0.16
D	12.00 BSC		
D1	10.00 BSC		
E	12.00 BSC		
E1	10.00 BSC		
e	0.80 BSC		
b	0.30	0.37	0.45
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:

- JEDEC OUTLINE : MS-026 BCB
- DIMENSIONS $D1$ AND $E1$ DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. $D1$ AND $E1$ ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

7.2.2. LQFP48



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	9.00 BSC		
D1	7.00 BSC		
E	9.00 BSC		
E1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:

1. JEDEC OUTLINE : MS-026 BBC
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

8. DISCLAIMER

The information appearing in this publication is believed to be accurate. Integrated circuits sold by Generalplus Technology are covered by the warranty and patent indemnification provisions stipulated in the terms of sale only. GENERALPLUS makes no warranty, express, statutory implied or by description regarding the information in this publication or regarding the freedom of the described chip(s) from patent infringement. FURTHERMORE, GENERALPLUS MAKES NO WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PURPOSE. GENERALPLUS reserves the right to halt production or alter the specifications and prices at any time without notice. Accordingly, the reader is cautioned to verify that the data sheets and other information in this publication are current before placing orders. Products described herein are intended for use in normal commercial applications. Applications involving unusual environmental or reliability requirements, e.g. military equipment or medical life support equipment, are specifically not recommended without additional processing by GENERALPLUS for such applications.

9. REVISION HISTORY

Date	Revision #	Description	Page
Mar. 08, 2024	1.3	1. Modify I/O Total MAX Current. 2. Modify SPI Timing Specifications.	24, 16
Jan. 31, 2023	1.2	1. Modify SCK max frequency. 2. Modify Operating voltage. 3. Remove the maximum number of LED driver. 4. Add "LQFP48 Thermal resistance Junction to Case" and "LQFP48 Thermal resistance Junction to Ambient" to section 6.2.	4,15, 23
Aug. 17, 2022	1.1	1. The address of 1BH is corrected to 13H in section 5.2.4. 2. Register 1BH's B6~B4 is corrected to PA_DIV2~0, register 1BH's B2~B0 is corrected to PC_DIV2~0 in section 5.2.3.	12, 13
Mar. 08, 2022	1.0	Original	28
Dec. 02, 2021	0.1	Preliminary version	27